In the claims:

1. (currently amended) A method for forming ultra shallow junctions, comprising:

providing a semiconductor;

implanting a dopant species into said semiconductor; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1050°C to 1350°C for from about 0.5 to about 3 milliseconds.

2. (previously presented) The method of claim 1 further comprising an amorphizing implant.

3. (previously presented) The method of claim 2 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

4. (canceled)

5. (currently amended) A method for forming junction in integrated circuits, comprising:

providing a semiconductor;

forming a patterned photoresist layer on said semiconductor;

implanting dopant species into said semiconductor;

removing said patterned photoresist layer;

annealing said implanted semiconductor with a solid phase epitaxy anneal; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C for from about 0.5 to about 3 milliseconds.

6. (canceled).

7. (previously presented) The method of claim 6 further comprising an amorphizing implant.

8. (previously presented) The method of claim 7 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

9. (currently amended) A method of forming a MOS transistor, comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on said semiconductor;

forming a gate electrode on said gate dielectric layer;

implanting dopant species into said semiconductor adjacent to said gate electrode;

annealing said implanted semiconductor with a solid phase epitaxy anneal at a temperature between 550°C and 950°C; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C for from about 0.5 to about 3 milliseconds.

10. (canceled)

11. (previously presented) The method of claim 10 further comprising an amorphizing implant performed prior to said implanting of said dopant species.

12. (previously presented) The method of claim 11 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

13. (currently amended) A method of forming an integrated circuit MOS transistor, comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on said semiconductor;

forming a gate electrode on said gate dielectric layer;

implanting first dopant species into said semiconductor adjacent to said gate electrode;

forming sidewall structures adjacent to said gate electrode;

implanting second dopant species into said semiconductor adjacent to said sidewall structures; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C for from about 0.5 to about 3 milliseconds.

14. (canceled)

15. (previously presented) The method of claim 14 further comprising an amorphizing implant performed prior to said implanting of said first dopant species.

16. (previously presented) The method of claim 15 further comprising an amorphizing implant performed prior to said implanting of said second dopant species.

17. (previously presented) The method of claim 13 further comprising an amorphous implant performed prior to said implanting of said second dopant species.

18. (previously presented) The method of claim 16 wherein said amorphizing implants comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.